REMARKS

This is a full and timely response to the outstanding Office Action mailed September 16, 2002. Reconsideration and allowance of the application and presently pending claims 1-19, as amended, are respectfully requested.

1. **Present Status of Patent Application**

Upon entry of this response, claims 1-19 remain pending in the present application. Specifically, claims 1, 2, 13 and 19 have been directly amended. The amendments are specifically described hereinafter. It is believed that the foregoing amendments add no new matter to the present application.

2. **Response to Objection to Drawings**

The Office Action states that "the drawings are objected to because...they fail to show Cjs as described in the specification." Applicant respectfully submits that C_{js} refers to the parasitic capacitance described in the background of the present application at page 3, line 22 through page 4, line 2. Thus, Applicant respectfully asserts that C_{js} is not part of the present invention and, therefore, is not included in FIG. 1. Applicant respectfully asserts that this objection should be withdrawn.

Furthermore, the Office Action asserts that "Sheet 6, line 11 compares Figure 1 to another Figure 1," and that "it is unclear to the Examiner if there should be other Drawings with this Application." Applicant respectfully submits that the foregoing amendments have corrected this error by replacing the final reference to Figure 1 with a

reference to previous circuits, and that there are no missing drawings with respect to the application.

3. **Response to Objection to Specification**

The Office Action states that "the specification is replete with terms which are not clear, concise and exact...examples of some unclear, inexact or verbose terms used in the specification are: page 3, unclear word: page 6, line 15, entire phrase is unclear, line 11, reference to Figure 1." With respect to page 3, Applicant has deleted the word "without" from line 9. With respect to the objection to page 6, line 11, the paragraph has been corrected to clarify that it refers to a comparison to previous ESD circuits. Finally, with regard to the objection to page 6, line 15, Applicant has amended the paragraph to add that a transmission line can couple the pad and the protected circuit as shown by FIG. 1. Applicant respectfully asserts that the specification of the present application is in compliance with 35 U.S.C. §112, first paragraph.

4. **Response to Rejection of Claims 1, 2, 4-7, 9, 10, 12-14, 16, 17 and 19 Under 35 U.S.C. §103(a)**

In the Office Action, claims 1, 2, 4-7, 9, 10, 12-14, 16, 17 and 19 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ravanelli (U.S. Patent 6,147,852) in view of Huard (U.S. Patent 4,875,130). It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements/features/stepsof the claim at issue. See,

e.g., *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

a. Claim 1

Claim 1 recites:

> 1. A circuit transferring a charge from a source to a reference potential, said circuit being placed between said source and a circuit to be protected, comprising:
> a transmission line coupling the source and the circuit to be protected;
> a transistor comprising a base, an emitter, and a collector; and
> an electrical ground; wherein
> **the transistor is directly connected in reverse mode between the electrical ground and the transmission line.**
> *(emphasis added)*

The Office Action asserts that "Ravanelli shows as part of Figure 1, a 'reverse mode' or reverse biased transistors Q1, Q2 connected in a diode configuration to form a 'Zener' diode combination." Applicant respectfully asserts that transistor Q2 of *Ravanelli* is not directly connected to electrical ground as claimed and that transistor Q1 is not connected in reverse mode. In stark contrast, *Ravanelli* FIG. 1 shows Q2 is connected between a transmission line and a resistor.

Further, the Office Action asserts that "Figure 2, further modifies on this principal, utilizing at least one bipolar transistor Q1 to shunt any ESD energy to a reference potential from an input circuit or a pad of a circuit to be protected, which may connect to an IC." However, *Ravanelli* FIG. 2, does not show a transistor directly connected in reverse mode between electrical ground and the transmission line. Applicant respectfully asserts that transistor Q1 is connected between Pad T1 and Supply T2, not ground.

With regard to the *Huard* reference, the Office Action states that "Huard discloses an ESD protection circuit, Figures 4 and 5, which utilizes collector-emitter "break-down" of a bipolar transistor 49 in response to current flowing across the reverse biased collector-base junction." Applicant respectfully asserts that "bipolar transistor 49" does not have a reverse biased collector base junction. In stark contrast to the assertion of the Office Action, bipolar transistor 49 operates in a forward bias, dissipating ESD from line 41 through transistor 49 to power supply 48. Thus, the current travels into the transistor through the collector and out of the transistor through the emitter. This is a typical forward bias.

Moreover, *Huard* does not disclose a transistor directly connected between a transmission line and ground. Instead, it merely shows a transistor connected between a power supply 48 and a diode 32. Therefore, neither reference shows a transistor in reverse mode directly connected between a transmission line and ground. Therefore, Applicant respectfully asserts that *Ravanelli* in view of *Huard* does not teach, disclose or suggest all of the elements/features of claim 1, and the rejection should be withdrawn.

b. Claim 2

Because independent claim 1 is believed to be allowable over the prior art of record, dependent claim 2 (which depends from independent claim 1) is allowable as a matter of law for at least the reason that the dependent claim 2 contains all features/elements of independent claim 1. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Moreover, claim 2 recites additional elements/features which are not shown in the cited references. For example, neither of the cited references shows the emitter of a transistor being connected to a transmission line, and neither of the cited references shows a collector being connected to electrical ground. Thus, there are other reasons why

this claim is allowable. The amendments made to this claim were made for the purpose of correcting an error submitted in the original claims. This amendment should have no effect on the patentability of claim 2 in light of the cited references.

c. Claim 4-7, 9, 10 and 12

Because independent claim 1 is believed to be allowable over the prior art of record, dependent claims 4-7, 9, 10 and 12 (which depend from independent claim 1) are allowable as a matter of law for at least the reason that the dependent claims 4-7, 9, 10 and 12 contain all features/elements of independent claim 1.

d. Claim 13

Claim 13 recites:

> 13. A method of protecting a circuit from an electrostatic discharge comprising:
> providing a bipolar junction transistor; and
> coupling said transistor between the circuit and a pad coupled to the circuit, wherein,
> **said transistor is configured in reverse mode, the collector of said transistor being connected directly to ground.**
> *(emphasis added)*

The Office Action asserts that "Ravanelli shows as part of Figure 1, a 'reverse mode' or reverse biased transistors Q1, Q2 connected in a diode configuration to form a 'Zener' diode combination." Applicant respectfully asserts that transistor Q2 of *Ravanelli* is not directly connected to electrical ground as claimed and that transistor Q1 is not connected in reverse mode. In stark contrast, *Ravanelli* FIG. 1 shows Q2 is connected between a transmission line and a resistor.

Further, the Office Action asserts that "Figure 2, further modifies on this principal, utilizing at least one bipolar transistor Q1 to shunt any ESD energy to a reference potential

from an input circuit or a pad of a circuit to be protected, which may connect to an IC." However, *Ravanelli* FIG. 2, does not show a transistor directly connected in reverse mode between electrical ground and the transmission line. Applicant respectfully asserts that transistor Q1 is connected between Pad T1 and Supply T2, not ground.

With regard to the *Huard* reference, the Office Action states that "Huard discloses an ESD protection circuit, Figures 4 and 5, which utilizes collector-emitter "break-down" of a bipolar transistor 49 in response to current flowing across the reverse biased collector-base junction." Applicant respectfully asserts that "bipolar transistor 49" does not have a reverse biased collector base junction. In stark contrast to the assertion of the Office Action, bipolar transistor 49 operates in a forward bias, dissipating ESD from line 41 through transistor 49 to power supply 48. Thus, the current travels into the transistor through the collector and out of the transistor through the emitter. This is a typical forward bias.

Moreover, *Huard* does not disclose a transistor directly connected between a transmission line and ground. Instead, it merely shows a transistor connected between a power supply 48 and a diode 32. Therefore, neither reference shows a transistor in reverse mode directly connected between a transmission line and ground. Therefore, Applicant respectfully asserts that *Ravanelli* in view of *Huard* does not teach, disclose or suggest all of the elements/features of claim 13, and the rejection should be withdrawn.

e. Claims 14, 16 and 17

Because independent claim 13 is believed to be allowable over the prior art of record, dependent claims 14, 16 and 17 (which depend from independent claim 13) are allowable as a matter of law for at least the reason that the dependent claims 14, 16 and 17 contain all features/steps of independent claim 13.

f. Claim 19

Claim 19 recites:

> 19. A circuit transferring a charge from a source to a reference potential, said circuit being placed between said source and a circuit to be protected, comprising:
> means for transmitting electromagnetic signals coupling the source and the circuit to be protected;
> means for switching electrical signals; and
> an electrical ground; wherein:
> **said switching means is directly connected in reverse mode between the electrical ground and said transmitting means.**
> *(emphasis added)*

The Office Action asserts that "Ravanelli shows as part of Figure 1, a 'reverse mode' or reverse biased transistors Q1, Q2 connected in a diode configuration to form a 'Zener' diode combination." Applicant respectfully asserts that transistor Q2 of *Ravanelli* is not directly connected to electrical ground as claimed and that transistor Q1 is not connected in reverse mode. In stark contrast, *Ravanelli* FIG. 1 shows Q2 is connected between a transmission line and a resistor.

Further, the Office Action asserts that "Figure 2, further modifies on this principal, utilizing at least one bipolar transistor Q1 to shunt any ESD energy to a reference potential from an input circuit or a pad of a circuit to be protected, which may connect to an IC." However, *Ravanelli* FIG. 2, does not show a switching means directly connected in reverse mode between electrical ground and the transmission line. Applicant respectfully asserts that transistor Q1 is connected between Pad T1 and Supply T2, not ground.

With regard to the *Huard* reference, the Office Action states that "Huard discloses an ESD protection circuit, Figures 4 and 5, which utilizes collector-emitter "break-down" of a bipolar transistor 49 in response to current flowing across the reverse biased collector-base

junction." Applicant respectfully asserts that "bipolar transistor 49" does not have a reverse biased collector base junction. In stark contrast to the assertion of the Office Action, bipolar transistor 49 operates in a forward bias, dissipating ESD from line 41 through transistor 49 to power supply 48. Thus, the current travels into the transistor through the collector and out of the transistor through the emitter. This is a typical forward bias.

Moreover, *Huard* does not disclose a switching means directly connected between a transmission line and ground. Instead, it merely shows a transistor connected between a power supply 48 and a diode 32. Therefore, neither reference shows a switching means in reverse mode directly connected between a transmission line and ground. Therefore, Applicant respectfully asserts that *Ravanelli* in view of *Huard* does not teach, disclose or suggest all of the elements/features of claim 19, and the rejection should be withdrawn.

5. **Response to Rejection of Claims 3, 11 and 15 Under 35 U.S.C. §103(a)**

In the Office Action, claims 3, 11 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Haas, Jr. et al.* (U.S. Patent 5,392,185), hereinafter *Haas I*, in view of *Ali* (U.S. Patent 6,292,046).

a. Claims 3 and 11

Because independent claim 1 is believed to be allowable over the prior art of record, dependent claims 3 and 11 (which depend from independent claim 1) are allowable as a matter of law for at least the reason that the dependent claims 3 and 11 contain all features/elements of independent claim 1.

b. Claim 15

Because independent claim 13 is believed to be allowable over the prior art of record, dependent claim 15 (which depends from independent claim 13) is allowable as a matter of law for at least the reason that the dependent claim 15 contains all features/elements of independent claim 13.

6. **Response to Rejection of Claims 8 and 18 Under 35 U.S.C. §103(a)**

In the Office Action, claims 8 and 18 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Haas, Jr. et al.* (U.S. Patent 5,537,284), hereinafter *Haas II.*

a. Claim 8

Because independent claim 1 is believed to be allowable over the prior art of record, dependent claim 8 (which depends from independent claim 1) is allowable as a matter of law for at least the reason that the dependent claim 8 contains all features/elements of independent claim 1.

b. Claim 18

Because independent claim 13 is believed to be allowable over the prior art of record, dependent claim 18 (which depends from independent claim 13) is allowable as a matter of law for at least the reason that the dependent claim 18 contains all features/elements of independent claim 13.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-19 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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ANNOTATED VERSION OF SPECIFICATION PARAGRAPHS SHOWING CHANGES

The following is a marked up version of the amended specification paragraphs. Amend the following paragraphs by adding the language that is underlined ("___") and by deleting the language that is enclosed within brackets ("[ ]"):

Please amend the paragraph beginning on page 2, line 23:

To prevent ESD from damaging semiconductor circuits, various protective schemes may be employed. Large-scale protective schemes are often used to protect system level equipment. Examples of these schemes include, but are not limited to, the following: electrical grounding of cases and external surfaces of the electrical equipment; electrical grounding of technicians via wrist bands; the prevention of electrostatic build-up through the use of static-safe clothing static control shoes and high humidification; and the use of specialized shipping containers and bags. All of the above methods help to prevent the build-up of static charge. Additionally, small-scale, chip specific, approaches may be used. Often, high-current clamping devices are placed on the pins of a chip so that the high currents associated with an ESD event are safely shunted [without]away from the circuitry.

Please amend the paragraph beginning on page 4, line 5:

Because ESD protection is just as important for high-frequency circuits as it is for lower-frequency circuits, there is a need for an on-chip ESD protection circuit that operates without adversely [effecting]affecting the performance of the high frequency circuit.

Please amend the paragraph beginning on page 6, line 7:

In **Figure 1**, the capacitance, C_{be}, between the base 208 and the emitter 204,[C_{be}] is indicated by capacitor 216. Because of the configuration of transistor 202, the value of C_{be} is approximately 10 times greater than the value of C_{js}. Thus, the high frequency performance is much improved. Thus, the response at high frequencies is greatly improved as compared to [the circuit of Figure 1]previous circuits.

Please amend the paragraph beginning on page 6, line 12:

The present invention thus provides for a method for protecting a circuit from electrostatic discharges through the connection of a transistor in the reverse mode between a protected circuit and a pad coupled to the protected circuit, where the pad couples the protected circuit to, for example, a transmission line.

ANNOTATED VERSION OF CLAIMS SHOWING CHANGES

The following is a marked up version of the amended claims. Amend the following claims by adding the language that is underlined ("___") and by deleting the language that is enclosed within brackets ("[ ]"):

1. (Once Amended) A circuit transferring a charge from a source to a reference potential, said circuit being placed between said source and a circuit to be protected, comprising:

a transmission line coupling the source and the circuit to be protected;

a transistor comprising a base, an emitter, and a collector; and

an electrical ground; wherein

the transistor is directly connected in reverse mode between the electrical ground and the transmission line.

2. (Once Amended) The circuit of claim 1, wherein said transistor is an *npn* transistor, the collector of said transistor is [coupled]connected to the electrical ground, the base of said transistor is coupled to the electrical ground, and the emitter of said transistor is [coupled between the electrical ground and]connected to the transmission line.

13. (Once Amended) A method of protecting a circuit from an electrostatic discharge comprising:

providing a bipolar junction transistor; and

coupling said transistor between the circuit and a pad coupled to the circuit, wherein,

said transistor is configured in reverse mode, the collector of said transistor being connected directly to ground.

19. (Once Amended) A circuit transferring a charge from a source to a reference potential, said circuit being placed between said source and a circuit to be protected, comprising:

means for transmitting electromagnetic signals coupling the source and the circuit to be protected;

means for switching electrical signals; and

an electrical ground; wherein:

said switching means is directly connected in reverse mode between the electrical ground and said transmitting means.